Tomoyuki Nakabayashi
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Education

Ph.D. Student in Engineering, Mie University, April 2011-Present

M.E. in Information Engineering, Mie University, April 2009-March 2011.

B.E. in Information Engineering, Mie University, April 2005-March 2009.

Research Interest

Energy-efficient microprocessor architecture, low-power VLSI design, glitch elimination, low-power D-Flip Flop, true-single-phase clocking circuit design, multi core architecture.

Research projects

Variable Stages Pipeline (VSP): In order to achieve high energy-efficient computing, we develop VSP that dynamically varies the pipeline depth.

- **Low-energy technique for VSP, Spring 2008-Spring 2009**
  Developed low-energy technique that improves the performance of a VSP.
- **Fabricate a VSP chip, Spring 2008-Spring 2010**
  Fabricated a VSP chip on a Rohm 180nm CMOS technology and measured energy consumption using by LSI tester.
- **Controller for VSP processor, Spring 2011-Present**
  Developed a controller for VSP processor that can reduce the energy consumption at several hundred clock cycles.

Alpha compatible processor, Fall 2009-Present
Developing Alpha compatible out-of-order superscalar processor.

Low-power D-FF, December 2010-Present
Developed two low-power D-FFs that can reduce more delay and power consumption than conventional D-FF.

Experience

Teaching assistant, April 2009-January 2010, April 2011-Present.
Dept. of Information Engineering, Mie University. Instruct and supervise information engineering laboratory that is to study computer architecture by designing a MIPS subset processor using Mentor Graphics ModelSim and Altera's

FPGA.

Intern, Panasonic Corporation, August 2009.
Development of management tool of Verilog simulation results by using Direct Programming Interface-C that interface between System Verilog and C language.

Publications

Academic paper

Nakabayashi, T., Sasaki, T., Ohno, K. and Kondo, T.: 'Design and Evaluation of Variable Stages Pipeline Processor with Low Energy Techniques', IET Journal of Computers and Digital Techniques, (Accepted).

Nakabayashi, T., Sasaki, T., Ohno, K. and Kondo, T.: 'Low Energy Techniques for Variable Stages Pipeline Focused on Clock System Power', IEICE Journal of Information and System Society, Vol. J94-D, No. 4, April, 2011 (Japanese).

International conference

Nakabayashi, T., Sasaki, T., Ohno, K. and Kondo, T.: 'Low Power Semistatic TSPC D-FFs Using Split-output Latch', Proc. of Int. SoC Design Conf., November 2011.

Nakabayashi, T., Sasaki, T., Ohno, K. and Kondo, T.: 'Design and Evaluation of Variable Stages Pipeline Processor Chip', Proc. of Asia and South Pacific Design Automation Conference (ASP-DAC2011), University Design Contest-1D-12, January, 2011.

Nakabayashi, T., Sasaki, T., Ohno, K. and Kondo, T.: 'Design and Evaluation of Variable Stages Pipeline Processor Chip', Proc. of Int. Symposium on Information and Automation, November 2010.

Sasaki, T., Nomura, K., **Nakabayashi, T.**, Ohno, K. and Kondo, T.: 'Fine Grain Controller for Variable Stages Pipeline Processor', International Technical Conference on Circuits/Systems, Computers and Communications, July, 2010, pp. 748-751.

Technical skills

Programming languages: C, Assembly(Alpha ISA, MIPS ISA), Verilog HDL, System Verilog, SPICE.

Tools: Synopsys (vcs, DesignCompiler, PrimeTime, Astro, HSPICE, nanosim),

Cadence (Virtuoso).